UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,031	03/26/2004	Xiaodong Jin	MP0358/13361-058001	1354

26200 7590 08/05/2008
FISH & RICHARDSON P.C.
P.O BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
BAUER, SCOTT ALLEN	
ART UNIT	PAPER NUMBER
2836	
MAIL DATE	DELIVERY MODE
08/05/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/811,031
Filing Date: March 26, 2004
Appellant(s): JIN ET AL.

Christina Jordan (Reg. No. 58,720)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 04/04/2008 appealing from the Office action mailed 09/24/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,738,248	JENKINS	5-2004
5,994,760	DUCLOS	11-1999
WO 02/05380	RUTFORS ET AL.	1-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5, 8-11, 13, & 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenkins et al. (US 6,738,248) in view of Duclos (US 5,994,760) and Rutfors (WO 02/05380).

With regard to Claim 1, Jenkins et al., in Figure 1, discloses a low noise amplifier (100), comprising: an input (104); and an electrostatic discharge protection circuit

including (108), a pair of diodes (D1 & D2) each having a first and a second terminal; a first diode (D1) of the pair having a first terminal coupled to the radio frequency input (104) and a second terminal directly coupled to a first supply (VSS); a second diode (D2) of the pair having a second terminal coupled to the radio frequency input (104) and a first terminal directly coupled to the first supply (VSS); the electrostatic discharge protection circuit operable to shunt electrostatic discharge current during positive and negative electrostatic discharge events away from the radio frequency input and through the first supply (column 3 lines 34-53).

Jenkins et al. does not teach that the input in a radio frequency input, or that a separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event.

Rutfors et al., in fig. 7 teaches a low noise amplifier (335) coupled to a radio frequency input.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Rutfors, by incorporating the protection of Jenkins into the device of Rutfors et al., for the purpose of providing ESD protection to a wireless circuit thus preventing the LNA from being damaged.

Further, It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed

apparatus from the prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham, 2 USPQ2d 1647 (1987).*

Duclos, in Figure 2, teaches an electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event (column 1 lines 49-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Duclos, by incorporating the device of Duclos between the terminals VDD and VSS of Jenkins et al., for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply (column 1 lines 36-39).

With regard to Claim 9, Jenkins et al., in Figure 1, discloses a low noise amplifier (100), comprising: receiving means for receiving an RF input (104); and shunting means (108) including, a pair of diode means (D1 & D2) each having a first terminal and a second terminal; a first diode means (D1) of the pair having a first terminal coupled to the receiving means and a second terminal directly coupled to a first supply; a second diode means (D2) of the pair having a second terminal coupled to the receiving means and a first terminal coupled directly to the first supply; and the shunting means for shunting electrostatic discharge current during positive and negative electrostatic discharge events away from the receiving means and through the first supply (VSS) (column 3 lines 34-53).

Jenkins et al. does not teach that the receiving means is for receiving an RF input, or that a separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event.

Rutfors et al., in fig. 7 teaches a low noise amplifier (335) coupled to a radio frequency input such that it receives an RF input.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Rutfors, by incorporating the protection of Jenkins into the device of Rutfors et al., for the purpose of providing ESD protection to a wireless circuit thus preventing the LNA from being damaged.

Further, It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from the prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham, 2 USPQ2d 1647 (1987).*

Duclos, in Figure 2, teaches an electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event (column 1 lines 49-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Duclos, by incorporating the device of Duclos between the terminals VDD and VSS of Jenkins et

al., for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply (column 1 lines 36-39).

With regard to Claims 2 & 10, Jenkins et al. in view of Duclos and Rutfors et al. discloses the low noise amplifier of Claims 1 & 9 wherein the first and second diodes are formed by one of polymer devices and metal oxide silicon devices. (column 3, lines 27-33).

With regard to Claims 3 &11 Jenkins et al. in view of Duclos and Rutfors et al., in Figure 1, discloses the low noise amplifier of Claims 1 & 9, wherein the first supply is one of a low voltage supply and a high voltage supply, and if the first supply is a low voltage, then the electrostatic discharge protection circuit is not directly coupled to a corresponding high voltage supply, if the first supply is a high voltage supply, then the electrostatic discharge protection circuit is not directly coupled to a corresponding low voltage supply.

With regard to Claims 5 & 13, Jenkins et al. in view of Duclos and Rutfors et al., in Figure 1, discloses the low noise amplifier of Claims 3 & 11 wherein the positive and negative electrostatic discharge events necessarily include a radio frequency input to high voltage supply positive discharge pulse, a radio frequency input to high voltage supply negative discharge pulse, a radio frequency input to low voltage supply positive

discharge pulse, and a radio frequency input to low voltage supply negative discharge pulse.

With regard to Claims 8 & 16, Jenkins et al. in view of Duclos and Rutfors et al. teaches the low noise amplifier of Claims 1 & 9. Jenkins et al. further teaches that the system is used in a high-speed communication circuit (column 2 lines 37-40). Rutfors et al. also teaches that the system is a wireless system.

Jenkins et al. does not teach that the low noise amplifier is compliant with an IEEE standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, and 802.11i, and 802.14.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that a device used in a high speed communication circuit would necessarily be compliant with IEEE standards as the interference created by the device would prevent components that the device relies upon from working properly and to enable the high speed communication circuit to operate and comply with standard industry-wide safety requirements.

Claims 17-19, 21, 24-26, 28, 31, 32 & 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenkins et al. (US 6,738,248) in view of Duclos (US 5,994,760).

With regard to Claim 17, Jenkins et al., in Figure 1, discloses an electrostatic discharge protection circuit (300), comprising: a pair of diodes (D1 & D2) each having a first terminal and a second terminal; a first diode (D1) of the pair having a first terminal coupled to an input/output pad and a second terminal directly coupled to a first supply; a second diode (D2) of the pair having a second terminal coupled to the input/output pad (104) and a first terminal directly coupled to the first supply; and the electrostatic discharge protection circuit operable to shunt electrostatic discharge current during positive and negative electrostatic discharge events (column 1 lines 36-39).

Jenkins et al. does not teach a separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event.

Duclos, in Figure 2, teaches an electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event (column 1 lines 49-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Duclos, by incorporating the device of Duclos between the terminals VDD and VSS of Jenkins et al., for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply (column 1 lines 36-39).

With regard to Claim 24, Jenkins et al., in Figure 1, discloses an electrostatic discharge protection circuit (300) for discharging electrostatic discharge events,

comprising: shunting means (108) including, a pair of diode means having a first terminal and a second terminal; a first diode means (D1) of the pair having a first terminal directly coupled to an input/output pad (104) a second terminal coupled to a first supply; and a second diode means (D2) of the pair having a second terminal coupled to the input/output pad and a first terminal directly coupled to the first supply; and the shunting means for shunting electrostatic discharge current during positive and negative electrostatic discharge events.

Jenkins et al. does not teach a separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event.

Duclos, in Figure 2, teaches an electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event (column 1 lines 49-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Duclos, by incorporating the device of Duclos between the terminals VDD and VSS of Jenkins et al., for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply (column 1 lines 36-39).

With regard to Claim 31, Jenkins et al., in Figure 1, discloses a method for discharging electrostatic discharge, comprising: providing a first direct discharge path between an input/output pad and a first supply; providing a second direct discharge path

between the input/output pad and the first supply; and shunting electrostatic discharge current during positive and negative electrostatic discharge events through one of the first discharge path and the second discharge path.

Jenkins et al. does not teach providing a third discharge path between the first supply and a second supply during an electrostatic discharge event.

Duclos, in Figure 2, teaches an electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event (column 1 lines 49-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Duclos, by incorporating the device of Duclos between the terminals VDD and VSS of Jenkins et al., for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply (column 1 lines 36-39).

With regard to Claims 18, & 25, Jenkins et al. in view of Duclos discloses the low noise amplifier of Claims 24 & 31, wherein the first and second diodes are formed by one of polymer devices and metal oxide silicon devices (column 3, lines 27-33).

With regard to Claims 19, 26 & 32, Jenkins et al. in view of Duclos, in Figure 1, discloses the low noise amplifier of Claims 17, 24 & 31, wherein the first supply is one of

a low voltage supply and a high voltage supply, and if the first supply is a low voltage, then the electrostatic discharge protection circuit is not directly coupled to a corresponding high voltage supply, if the first supply is a high voltage supply, then the electrostatic discharge protection circuit is not directly coupled to a corresponding low voltage supply.

With regard to Claims 21, 28 & 34, Jenkins et al. in view of Duclos, in Figure 1, discloses the low noise amplifier of Claims 19, 26 & 32 wherein the positive and negative electrostatic discharge events necessarily include a radio frequency input to high voltage supply positive discharge pulse, a radio frequency input to high voltage supply negative discharge pulse, a radio frequency input to low voltage supply positive discharge pulse, and a radio frequency input to low voltage supply negative discharge pulse.

Allowable Subject Matter

Claims 6 & 14, would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because the prior art of record does not teach or fairly suggest an apparatus comprising all the features as recited in the claims and in combination with the low voltage supply floating during the radio frequency input to high voltage supply positive discharge pulse and the radio frequency input to high voltage supply negative discharge pulse.

Claims 7 & 15 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because the prior art of record does not teach or fairly suggest an apparatus comprising all the features as recited in the claims and in combination with the high voltage supply floating during the radio frequency input to low voltage supply positive discharge pulse and the radio frequency input to low voltage supply negative discharge pulse.

Claims 22, 29 & 35 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because the prior art of record does not teach or fairly suggest a low noise amplifier comprising all the features as recited in the claims and in combination with wherein the low voltage supply floating during the radio frequency input to high voltage supply positive discharge pulse and the radio frequency input to high voltage supply negative discharge pulse.

Claims 23, 30 & 36 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because the prior art of record does not teach or fairly suggest a low noise amplifier comprising all the features as recited in the claims and in combination with the high voltage supply necessarily floats during the radio frequency input to low voltage supply positive discharge pulse and the radio frequency input to low voltage supply negative discharge pulse.

(10) Response to Argument

With regard to claim 1, Appellant initially argues the combination of Jenkins and Duclos, stating that there is no reason to combine the two references. Appellant argues that there is no reason to combine the two references by placing the rail to rail diode clamps found in Fig. 2 of Duclos, between the VDD and VSS terminals into the embodiment found in Fig. 1 of Jenkins. Appellant argues that a third embodiment of Jenkins teaches a way to protect against ESD events that occur between VDD and VSS and thus there is no reason to place additional an ESD protection clamp between the two power supply voltages as this would duplicate the existing protection.

Initially, it is pointed out that the embodiment of Jenkins' Fig. 3 is not relied upon and only the embodiment found in Fig. 1 is used to reject all currently rejected claims. In Fig. 1, Jenkins teaches a circuit that has no protection between lines VDD and VSS. Jenkins provides bidirectional ESD protection between an input signal and VSS. This embodiment provides no VDD to VSS protection against ESD and thus, the addition of the clamp taught by Duclos would not duplicate any protection already provided. The fact that Jenkins provides a method of protecting against ESD occurring between VDD and VSS in an embodiment that is not relied upon does not mean that an improved method of clamping between VDD and VSS cannot be applied to the embodiment of Fig.1. The clamp of Fig.3 of Jenkins contains two deficiencies compared to the clamp of Duclos. First, a clamp that is connected as taught in Fig. 3 of Jenkins requires that two voltage drops across diodes D2 and D6 must be reached before an ESD event can be shunted. This can increase the risk that the signal input can damage the buffer as

the transient voltage must be one voltage drop higher to trigger the protection circuit. The second disadvantage is that Fig. 3 of Jenkins does not provide bidirectional protection between VDD and VSS. If a large negative ESD event occurs between VDD and VSS or the power lines are mistakenly wire in reverse, there would be no path to clamp the two rails together, short of placing the diodes in a reverse breakdown condition which would permanently damage the diodes. By placing the clamp of Duclos between the VDD and VSS lines of Jenkins' Fig.1, both of these problems are solved. To summarize, the rejection does not place the clamp of Duclos in parallel with the diodes D5 and D6 of Jenkins' Fig. 3. Rather the clamp of Duclos is placed in parallel with the input buffer of Jenkins' Fig. 1. In no embodiment does Jenkins disclose bidirectional protection between VDD and VSS and thus, one of ordinary skill in the art interested in protection against both positive and negative ESD events occurring from the positive rail to the negative rail would have been motivated to combine the two references as described.

Applicant next argues the combinability of Jenkins with Rutfors and states that motivation has not been provided for combining the two references. One of ordinary skill in the art would recognize that the protection arrangement of Jenkins relates to communications circuitry and could be used for a wide array of electrical devices used in communications circuitry. This allows the protection circuit to be more robust, opening the circuit to a greater market and allowing a larger number of devices to be sold. Further, as stated in the previous action, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does

not differentiate the claimed apparatus from the prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham, 2 USPQ2d 1647 (1987).*

Appellant next argues the rejection of claims 6 & 7. These arguments are moot as the claims in question have been indicated as being allowable if rewritten to contain all the limitations of the base claim and any other intervening claims as stated in the previous final rejection.

The arguments of the remaining independent claims 9, 17, 24 and 31 are similar in nature to the arguments of claim 1 and thus have already been addressed.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/SAB/

20 JUL 08

/Michael J Sherry/

Supervisory Patent Examiner, Art Unit 2836

Conferees:

/Michael J Sherry/

Supervisory Patent Examiner, Art Unit 2836

/David S Blum/

TQAS Appeal Specialist, TC 2800